CTTT

Technical Design Report

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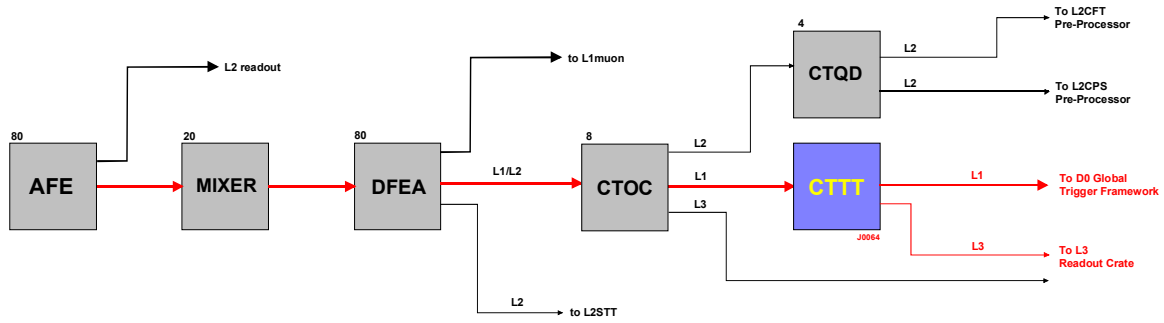
1. INTRODUCTION

The CTTT board is the final 'concentrator' board in the CTT system [1]. It collects CFT and CPS axial information from all eighty sectors and uses this data to make simple trigger bits, which are passed on to the trigger framework. The CTTT board gets the following data from eight CTOC boards:

- Counts of CFT tracks with no CPS cluster match
- Counts of CFT tracks with CPS cluster match
- Count of CPS clusters
- Doublet occupancy
- Isolated CFT tracks
- Sum of |pT|

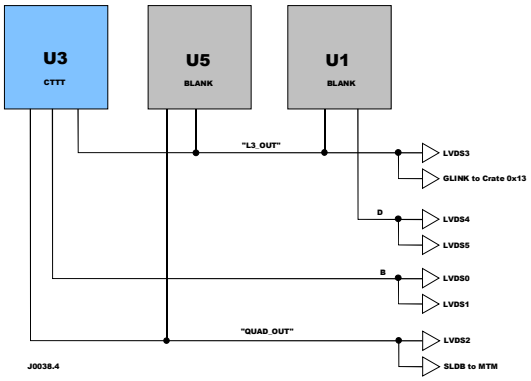
The CTTT also has a L3 sender, which allows the CTTT to dump out the L1 records for a specific crossing in response to a L1_ACCEPT signal. To further assist in debugging the system the CTTT provides status information about the input links, and a mechanism is provided to inject test vectors into the output data stream going to the trigger framework.

2. L1CTT CHAIN DIAGRAM



The output of the CTTT is sent to the trigger framework via a Muon Trigger Manager crate. The CTTT's L3 output is fed into readout crate 0x13.

3. CTTT BUS STRUCTURE



There are three FPGAs on the CTTT daughterboard, however only U3 (device 0) is used; the other two FPGAs must be loaded with 'blank' firmware files. Device U3 is a Xilinx Virtex FPGA model XCV600-4BG432C.

4. RECORD TYPES AND DEFINITIONS

4.1. CTTT INPUT RECORDS

The CTTT expects the CTOC to continuously send L1 records following the Protocols Document [2]. The L1Accept control bit is not present in the normal L1 records coming from the CTOC – and the CTTT needs to know when a L1accept occurs so that it can transmit its L3 record. To accomplish this, the CTOC sends a "dummy" L2 record to the CTTT board when a L1accept occurs. Refer to the L1CTOC Technical Design Report [3] for details.

4.2. CTTT TRIGGER TERMS (NEOTERMS)

These trigger terms are indexed by "neoterm" numbers. These neoterms are packed into the SLDB output record as follows:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
3	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
4	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
5	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
6	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
7	Vertial Parity															

[0]	**Pass-N-Mark**	Currently used only for debugging purposes.
[1]	**TTK(1, 1.5)**	One or more tracks above 1.5 GeV.
[2]	**TTK(1, 3)**	One or more tracks above 3 GeV.
[3]	**TTK(1, 5)**	One or more tracks above 5 GeV.
[4]	**TTK(1, 10)**	One or more tracks above 10 GeV.
[5]	**TTK(2, 1.5)**	Two or more tracks above 1.5 GeV.
[6]	**TTK(2, 3)**	Two or more tracks above 3 GeV.
[7]	**TTK(2, 5)**	Two or more tracks above 5 GeV.
[8]	**TTK(2, 10)**	Two or more tracks above 10 GeV.
[9]	**TEL(1, 1.5)**	One or more tracks above 1.5 GeV with a tight CPS match.
[10]	**TEL(1, 3)**	One or more tracks above 3 GeV with a tight CPS match.
[11]	**TEL(1, 5)**	One or more tracks above 5 GeV with a tight CPS match.
[12]	**TEL(1, 10)**	One or more tracks above 10 GeV with a tight CPS match.
[13 – 34]	*reserved*	
[35]	**TIS(1, 5)**	One or more isolated tracks above 5 GeV.
[36]	**TIS(1, 10)**	One or more isolated tracks above 10 GeV.
[37, 38]	*reserved*	
[39]	**THT(5)**	Total CFT axial doublet occupancy is greater than ~5 %.
[40]	**THT(10)**	Total CFT axial doublet occupancy is greater than ~10 %.
[41]	**THT(20)**	Total CFT axial doublet occupancy is greater than ~20 %.
[42, 43]	*reserved*	
[44]	**TIQ(1, 5, 1)**	One or more isolated tracks in quadrant 1 with pT ≥ 5 GeV.
[45]	**TIQ(1, 5, 2)**	One or more isolated tracks in quadrant 2 with pT ≥ 5 GeV.
[46]	**TIQ(1, 5, 3)**	One or more isolated tracks in quadrant 3 with pT ≥ 5 GeV.
[47]	**TIQ(1, 5, 4)**	One or more isolated tracks in quadrant 4 with pT ≥ 5 GeV.
[48 - 53]	*reserved*	
[54]	**TIL**	"Golden Track". One or more isolated tracks in a sector with low doublet occupancy.
[55]	**TIS(2, 5)**	Two or more isolated tracks with pT ≥ 5 GeV.
[56]	**TIS(2, 10)**	Two or more isolated tracks with pT ≥ 10 GeV.
[57]	**TEL(2, 1.5)**	Two or more tracks with pT ≥ 1.5 GeV and a tight CPS cluster match.
[58]	**TEL(2, 3)**	Two or more tracks with pT ≥ 3 GeV and a tight CPS cluster match.
[59]	**TEL(2, 5)**	Two or more tracks with pT ≥ 5 GeV and a tight CPS cluster match.
[60]	**TEL(2, 10)**	Two or more tracks with pT ≥ 10 GeV and a tight CPS cluster match.
[61]	**TIS(2, 3)**	Two or more isolated tracks with pT ≥ 3 GeV.
[62]	**TES(2, 3)**	Two or more isolated tracks with pT ≥ 3 GeV and a tight CPS cluster match.
[63]	**TIS(1, 3)**	One or more isolated tracks with pT ≥ 3 GeV
[64]	**TES(1,1.5)**	One or more isolated tracks with pT ≥ 1.5 GeV and a tight CPS cluster match.
[65]	**TES(1, 3)**	One or more isolated tracks with pT ≥ 3 GeV and a tight CPS cluster match.
[66]	**TES(1, 5)**	One or more isolated tracks with pT ≥ 5 GeV and a tight CPS cluster match.
[67]	**TES(1, 10)**	One or more isolated tracks with pT ≥ 10 GeV and a tight CPS cluster match.
[68]	**TES(2, 1.5)**	Two or more isolated tracks with pT ≥ 1.5 GeV and a tight CPS cluster match.
[69]	**TES(2, 5)**	Two or more isolated tracks with pT ≥ 5 GeV and a tight CPS cluster match.
[70]	**TES(2, 10)**	Two or more isolated tracks with pT ≥ 10 GeV and a tight CPS cluster match.
[71 – 95]	*reserved*	

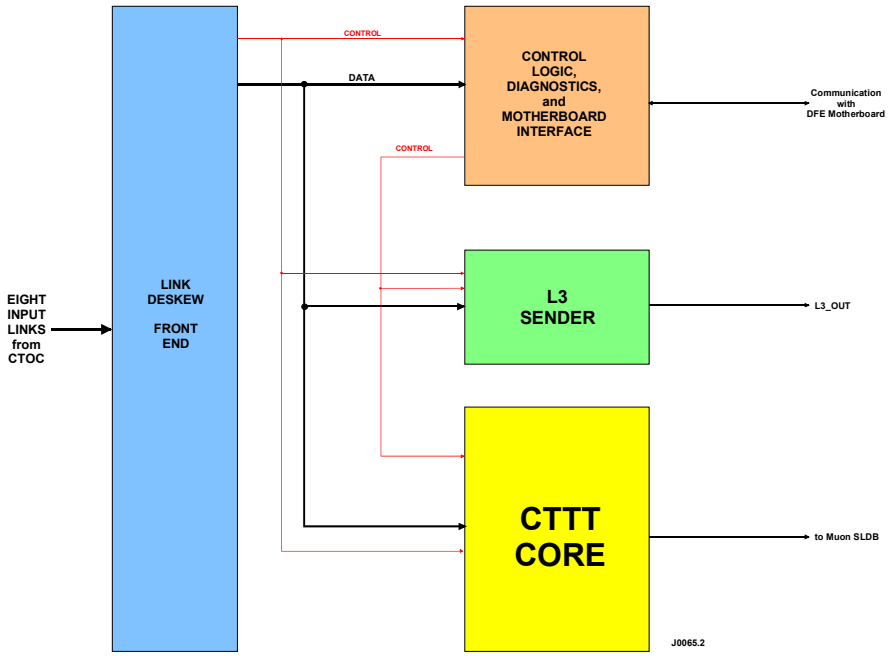
4.3. CTTT L3 OUTPUT

The CTTT transmits a L3 record when it receives a "dummy" L2 record from the CTOC board. This happens when a L1_ACCEPT occurs. The CTTT's L3 record follows the format specified in the Protocols Document [1]. The length of this record is fixed at 6 header + 8*14 data + 2 trailer = 120 16-bit words. The header fields are defined as:

```
HEADER_LENGTH = 0x03
#LVDS_IN-LINKS = 0x8
#DWORDS = 0x70
HDR_FORMAT = 010
OBJECT_FORMAT = 00001
L3_DATA_TYPE = 0x04
```

NOTE: the PARITY word at the end of the L3 record is set to 0x0000!

5. CTTT BLOCK DIAGRAM



5.1. LINK DESKEW FRONT END

The main purpose of the front end is to cleanly and reliably cross the link clock domains so that the rest of the design operates in the master clock domain. Small dual port rams are used as FIFOs to cross the clock domains. These dual port rams are constructed from distributed RAMs which are smaller than the true dual port BlockRAMs found on the Xilinx FPGAs. As a result, the distributed RAMs can be pushed closer to the input bus pins, thus reducing clock delays and clock skews on non-global clock nets (Links 3-9 use non-global clocks). The CTTT uses essentially the same front end as the L1CTOC design – refer to that Technical Design Report for technical details on how the front end works.

The outputs of the front end are:

1. Synchronized link data busses: **sync_link0[27..0]** through **sync_link7[27..0]**. These busses are copies of the input links realigned into the master clock domain.
2. The beginning of record (**BoR**) control signal, which marks the first timeslice.
3. **VALID_LINK(7..0)**. If a record header is not observed on an input within 64 clock cycles the front end asserts the corresponding bit in this bus. Its purpose is to mask off links which may be unplugged or otherwise damaged.

All outputs from the front end are synchronous to the master clock.

5.2. STATUS AND MOTHERBOARD INTERFACE

This module is responsible for checking the input links (after synchronization) for error conditions. It's also responsible for all communication with the DFE motherboard, DFE crate controller, and ultimately the online computers. Status information is sent back to the online computers, and through this module registers in the CTTT can be written after the CTTT is initialized.

5.2.1. Input Link Diagnostics

5.2.1.1. Synchronization Errors

When the front end asserts the BoR signal that means that each deskewed bus should be presenting the header frame. If this is not the case the corresponding sync_err[7:0] bit is set.

5.2.1.2. Parity Errors

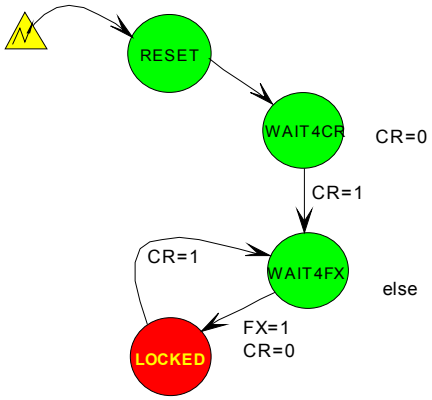
Each incoming L1 record has both horizontal and vertical parity bits. If there is a horizontal parity error in a L1 record the corresponding parity_err[7:0] bit is set. The vertical parity bits are not checked.

5.2.1.3. Pattern Errors

The CTOC can be placed in a test mode where it sends a special test pattern record to the CTTT. This test pattern record has been designed to have a normal L1 record header followed by a test pattern which tests all of the bits on the LVDS link. If the CTTT detects a bit error anywhere in this pattern it sets the corresponding bit in patt_err[7:0]. This feature is only intended for checking link integrity between the CTOC and the CTTT – don't try to do this when data taking!

5.2.2. Tick and Turn Counter

The CTTT needs to know the tick (crossing) and turn numbers so that it can insert these values into the L3 header and drive the control signals for the output link to the trigger framework. Based on the FX and CFT_RESET (CR) control bits received on link2 the counters are locked onto the incoming data stream. The tick and turn counter logic is based on the simplified state diagram:



CR happens infrequently (few times per hour) and is often asserted for a second or so. This active high signal is a global system reset (also called SCL_INIT). On the first FX after the CR goes low the counters are reset to turn=1, tick=7. The tick counter counts up to 158 and is then reset to zero, and the turn counter is incremented. If all is proceeding normally the tick and turn counter module will drive the LOCKED output high.

When the tick counter equals 6 it *expects* to see the next FX bit in the next L1 record. The tick and turn counter must be able to "ride out" a missing FX bit without dropping the LOCKED bit. If FX comes at an unexpected time, however, the tick and turn module will pulse the FX_Err output.

Both LOCKED and FX_err status bits are available to the outside world through the slow monitor interface.

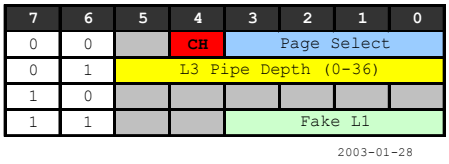
5.2.3. DFE MOTHERBOARD INTERFACE

5.2.3.1. SETTING PARAMETERS AFTER INITIALIZATION

After the CTTT board has been initialized, certain parameters may be changed dynamically, without re-initializing. These operations are:

- Change the current status page
- Clear history
- Set L3 pipeline depth
- Set fake mode bits

The DFE motherboard interface enables a single byte to be written to each FPGA on the CTTT daughterboard. The CTTT FPGA is device zero. The two upper bits of the byte select which register the lower 6 bits are written into:



This interface is **write only**, and it can be written at any time after the CTTT is initialized. Use the status pages (below) to read back CTTT status, including the values of these dynamic registers. The following dfe_ware macros show how to change some of the CTTT settings:

```
# clear the history bits and set current page to 0
# this is the safe way to do it, explicitly toggling it 0-1-0
set DFE 14
set device 0
cmd writebyte 3 0x00
cmd writebyte 3 0x10
cmd writebyte 3 0x00

# set the CTTT into fake mode 2, remember to set the two MSb's!
# 0x02 || 0xC0 = 0xC2
set DFE 14
set device 0
cmd writebyte 3 0xC2

# set the CTTT to pipeline depth 4
# 4 = 0x04, 0x04 || 0x40 = 0x44
set DFE 14
set device 0
cmd writebyte 3 0x44

# readback the current the L3 pipeline depth (page 3)
set DFE 14
set device 0
cmd writebyte 3 0x03
```

5.2.3.2. STATUS PAGES

The DFE motherboard interface allows one of the FPGAs on the board to continually send a status byte back to the DFE crate controller (DFEC). The DFEC makes this status byte available for reading by the online system computers. Since the CTTT has several bytes of status information to send back, a paged system is incorporated to send back one piece of data at a time.

page	S7	S6	S5	S4	S3	S2	S1	S0
0			FX Error	L2	Parity Err	Missing Link	Sync Err	TFW Locked
1								
2					Fake L1 Mode			
3			L3 Pipeline Depth [5..0]					
4								
5	0x55							
6	0xAA							
7								
8				Miss-link4	Miss-link3	Miss-link2	Miss-link1	Miss-link0
9						Miss-link7	Miss-link6	Miss-link5
10				Sync-err4	Sync-err3	Sync-err2	Sync-err1	Sync-err0
11						Sync-err7	Sync-err6	Sync-err5
12				Parity-err4	Parity-err3	Parity-err2	Parity-err1	Parity-err0
13						Parity-err7	Parity-err6	Parity-err5
14				Patt-err4	Patt-err3	Patt-err2	Patt-err1	Patt-err0
15						Patt-err7	Patt-err6	Patt-err5

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Orange colored cells are HISTORY bits. That means that if the bit is set, it remains set until explicitly cleared. This enables transient glitch conditions to be trapped and readout through a relatively slow interface.

FX Error: This bit is set if the FX control bit is missing or is arriving at unexpected times.
L2: This bit is set whenever the CTTT receives a "dummy" L2 record from the CTOC.
Parity Err: Logical OR of Parity-err[7:0]
Missing Link: logical OR of miss-link[7:0]
Sync_Err: logical OR of sync-err[7:0]
TFW Locked: Set to indicate that the tick and turn counter is happy with the incoming control bits and the tick and turn counters are incrementing normally.

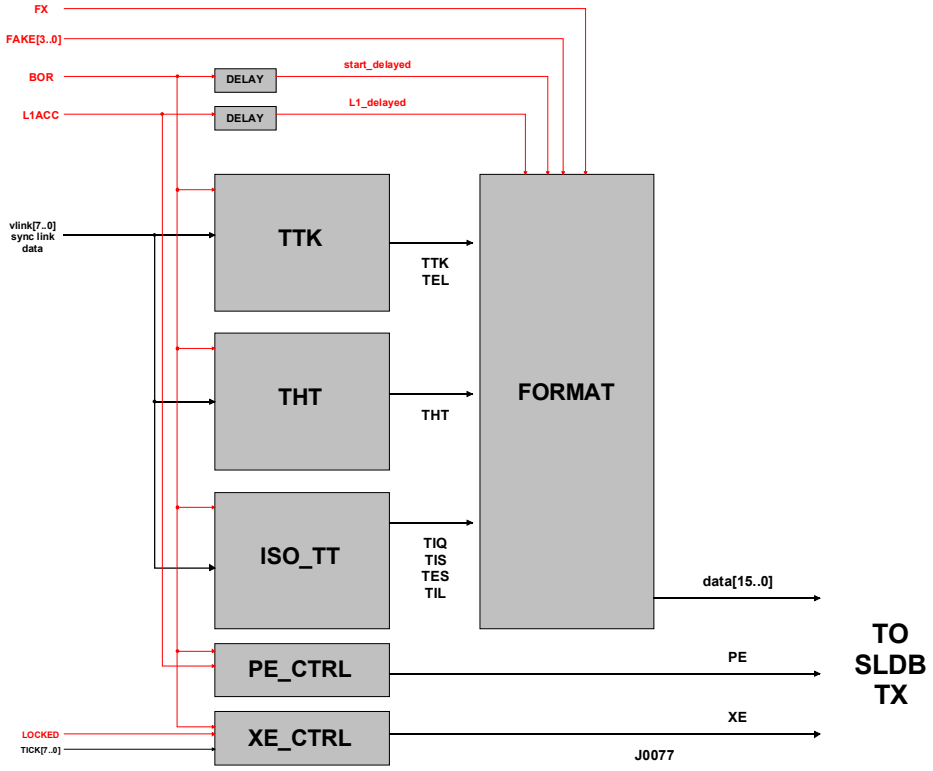
Fake_L1_Mode: Echoes back the fake register.
L3_Pipeline_Depth: Echos back the L3 pipeline depth register. Valid range is 0 to 36 crossings deep.
Pages 5, 6: Diagnostics, constant values.
Pages 8, 9: Missing-Link history bits. A bit is set if the corresponding input link has not seen a BoR signal in 64 clock cycles.
Pages 10, 11: Sync-Err history bits. A bit is set if the CTTT front end cannot properly deskew the incoming data and align it with the other links.
Pages 12, 13: Parity Error history bits. Set if a horizontal parity error is detected on an input link.
Pages 14, 15: Pattern Error bits. Set if a bit error is detected in the special L1 test pattern record sent by the CTOC.

5.3. L3 SENDER

The CTTT's L3 sender module is functionally identical to the L3 sender module in the L1CTOC design, except that it has been modified for 8 input links, not 10. The depth of the L3 pipeline is dynamically adjustable from 0 to 36 132ns crossings. (Setting the pipeline to zero will cause the CTOC's "dummy" L2 records to be reported in the L3 record.)

For a technical overview of the L3 sender logic, refer to the L1CTOC Technical Design Report [3].

5.4. CTTT CORE



Synchronized link data is fed into the TTK, THT, and ISO_TT modules, which calculate the trigger terms. If an input link does not have a corresponding vlink() bit set these modules will ignore that link's data. These modules are pipelined, and their trigger term outputs are stable for 7 clock cycles.

The BoR and L1accept signals are delayed so that they line up with the trigger term outputs of the TTK, THT, and ISO_TT modules.

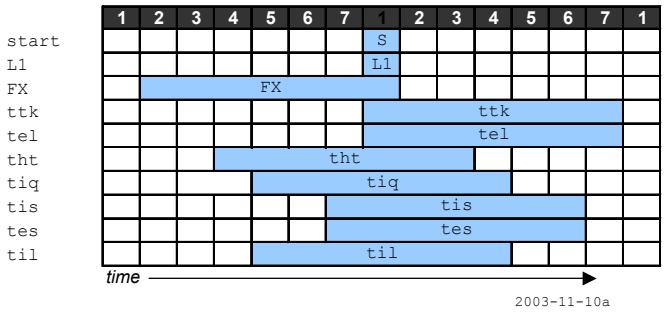
The format module waits for the delayed BoR signal (called start_delayed) and then loads the trigger terms into a shift register and clocks out 7 data frames to the Muon SLDB transmitter daughterboard. This daughterboard also requires a clock and two control bits: Parity Enable (PE) and Transmit Enable (XE).

Parity enable is always asserted on the last timeslice of the output record. Transmit Enable closely follows the beam structure, thus it relies on the tick and turn counter module in the front end to get the tick number. NOTE: If the tick and turn module looses LOCK then XE_CNTL module will not assert the Transmit Enable bit and the SLDB transmitter will not send any data to the trigger framework.

5.4.1. DATA ALIGNMENT INTO FORMATTER

The trigger term pipeline modules (TTK, THT, ISO_TT) hold their outputs stable for 7 clock cycles. However each pipeline has a different task, so the latency is different. This means that the trigger terms will arrive at the formatter module at different times. The formatter module waits until it gets the START bit, then it registers all of it's inputs and begins shifting out the data.

As it turns out the TTK and TEL pipelines have the longest latency, so the start and L1 control bits are delayed accordingly. The timing diagram below shows the relative timing of the data and control bits arriving at the formatter module.



The START bit is asserted 1 out of every 7 clock cycles, except when a "dummy" L2 record comes into the CTTT. After the "dummy" L2 record arrives at the CTTT there will be fairly long stretch of null frames, which the CTTT core "rides out" by sending empty output records to the SLDB transmitter. The CTTT's L1 transmission immediately resumes when the CTOC begins to send real L1 records.

5.4.1.1. DIAGNOSTIC (FAKE) OUTPUT RECORDS

In order to assist system level debugging the CTTT can replace it's normal L1 output record with fake data, depending on the value of the FAKE bits. The FAKE bits can be changed at any time by executing dfe_ware macros on the online cluster computers.

fake[3:0]	description
0000	normal data (reset default)
0001	set P&M bit every crossing
0010	set ttk(1,*) bit every crossing
0011	set nt[15:0] every crossing
1001	set P&M bit on first crossing
1010	set ttk(1,*) on first crossing
1011	set nt[15:0] on first crossing
others	send all zeros

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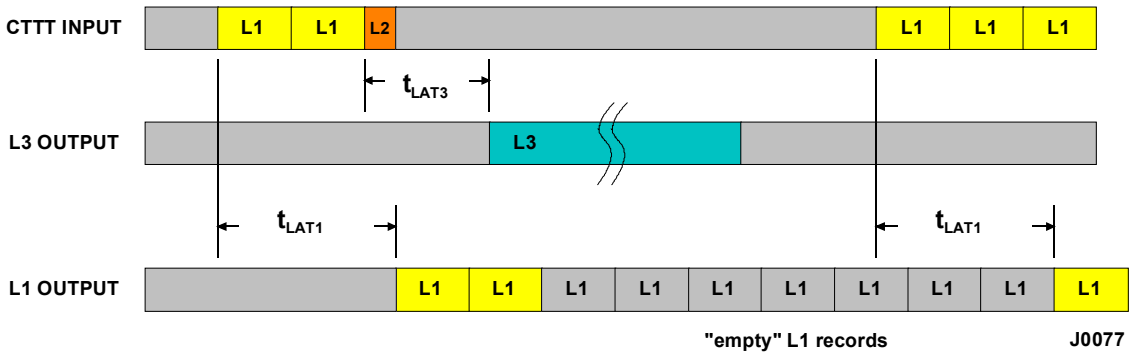
Note that the fake modes will only work correctly if the CTTT is happy with it's input data. Check to make sure that LOCKED is set and FX_ERR is cleared, otherwise most of the fake modes will send garbage to the trigger framework.

* note that in fake modes (1-3 and 9-11) the rest of the neoterms are zeroed out.

6. Timing and Latency



t_{LAT3} is the L3 latency, 9 clock cycles (169.2ns).
t_{LAT1} is the L1 latency, 17 clock cycles (319.6ns).

7. Device Resources

```
Device utilization summary:

   Number of External GCLKIOBs          4 out of 4     100%
   Number of External IOBs            291 out of 404    72%
      Number of LOCed External IOBs   291 out of 291   100%

   Number of BLOCKRAMs                 16 out of 24     66%
   Number of SLICEs                  2242 out of 6912   32%

   Number of GCLKs                      4 out of 4     100%
```

8. Revision History

000 4 September 2003: core algorithms only
001 4 September 2003: modify core algorihms, add stuff.
002 23 October 2003: add TIS(2,3), TES(2,3). All (2,x) terms now handle inclusiveness properly (“off diagonal”).
003 4 November 2003: reformat the trigger terms calculation page.
100 10 November 2003: added core diagrams, fake modes, motherboard interface and status pages.

9. References

1. J. Olsen et al., “The DØ Central Track Trigger,” IEEE Trans. Nucl. Sci., submitted for publication.

2. DFE Protocols Documentation:
http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs

3. J. Olsen, “L1CTOC Technical Design Report,” available online:
http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs